EXPRESS MAIL NO. EL872041338US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Present Application:

Applicants : Michael Nuttall and
Garry Anthony Mercaldi

Attorney Docket No. : 500803.02

Filed : Concurrently herewith

Title : METHOD FOR ENHANCING VERTICAL GROWTH DURING THE SELECTIVE FORMATION OF SILICON, AND STRUCTURES FORMED USING SAME

Prior Application:

Examiner : David Vu

Art Unit : 2818

Serial No. : 09/770,909

PRELIMINARY AMENDMENT

Box Patent Application
Commissioner of Patents
Washington, D.C. 20231

Sir:

In the Specification:

Amend the specification by inserting a new section before the "Technical Field" as follows:

-- CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of pending United States Patent Application No. 09/770,909, filed January 26, 2001. --

Please replace the paragraph beginning at page 2, line 13, with the following rewritten paragraph:

-- The lateral growth 118 may result in adjacent contacts undesirably touching each other, as indicated by the dotted lines 122 between the contacts 100 and 102. When the contacts 100 and 102 touch, an unwanted short circuit occurs and the devices being fabricated may not operate properly. As the size of devices being formed in integrated circuits continues to decrease, the distance between adjacent contacts 100, 102 and 102, 104 also decreases, making lateral growth 118 a concern since less lateral growth is required before adjacent contacts short circuit. While the amount of lateral growth of the contacts 100-104 can be reduced by forming the contacts for a shorter period of time, this is not a viable in most applications because the contacts must be formed to a desired height H, as indicated for the contact 100. As will be appreciated by those skilled in the art, the contacts 100-104 must reach the desired height H, for example, in order to ensure subsequent layers (not shown) can reliably connect to the contacts to provide electrical connection to the underlying devices. For example, in a MOS transistor it is desirable that contacts being formed to source and drain regions of the transistor are at least as high as a gate stack formed over a channel region of the transistor to ensure subsequent layers form proper connection to the contacts. --

Please replace the paragraph beginning at page 5, line 5, with the following rewritten paragraph:

-- During the selective formation of the contacts 200-204, the collimated electromagnetic radiation 208 is applied to the contacts to heat the horizontal upper surfaces of the contacts, as will be now described in more detail with reference to the contact 202. The contact 202 includes an upper surface 220 that is substantially horizontal or parallel to the upper surface on the silicon substrate 206, and further includes two sidewall surfaces 222 and 224 that are substantially vertical or perpendicular to the upper surface of the silicon substrate. The collimated electromagnetic radiation 208 has a direction of propagation, as indicated by the arrows, which is substantially perpendicular to the surface of the semiconductor substrate 206

and the upper surface 220. A scanning laser or other suitable source may be utilized to generate the collimated electromagnetic radiation 208, and although the radiation is described as being electromagnetic radiation, any directional radiation source that can heat the upper surface 220 by a relatively large amount compared to the sidewall surfaces 222, 224 can be utilized, as will be discussed in more detail below. --

Please replace the paragraph beginning at page 5, line 20, with the following rewritten paragraph:

-- Because the direction of propagation of the collimated electromagnetic radiation 208 incident on the upper surface 220 is substantially perpendicular to the upper surface, the intensity of the radiation incident upon the upper surface is relatively great, and thus the upper surface is heated by a relatively large amount due to the relatively high intensity of the applied electromagnetic radiation. As will be understood by those skilled in the art, the increased temperature of the upper surface 220 results in the deposition of more silicon on the upper surface. Thus, the increased temperature of the upper surface 220 due to the incident radiation 208 increases a vertical growth rate 226 of the contact 202 in the vertical direction indicated by the arrows. At the same time, the intensity of the radiation 208 incident upon the sidewall surfaces 222, 224 is relatively small compared to the intensity incident upon the upper surface 220. This is true because the sidewall surfaces 222, 224 are substantially vertical relative to the upper surface 220 and thus substantially parallel to the applied collimated electromagnetic radiation 208. As a result, a relatively small portion of the applied collimated electromagnetic radiation 208 is incident upon the sidewall surfaces 222, 224, and thus the surfaces are not significantly heated by the applied radiation. The sidewall surfaces 222, 224 are thus at a lower temperature relative to the upper surface 220. The lower temperature of the sidewall surfaces 222, 224 results in a lateral growth rate 228 in the horizontal direction as indicated by the arrows that is relatively small compared to the vertical growth rate 226. --

Please replace the paragraph beginning at page 7, line 17, with the following rewritten paragraph:

-- Figure 3 is a diagram illustrating a MOS transistor 300 formed in a semiconductor substrate 302, the MOS transistor including contacts 304, 306 formed according to the method of Figure 2. In the example of Figure 3, the MOS transistor is an NMOS device including an N+ source region 308 and N+ drain region 310, with a P-type channel 312 being defined between the source and drain regions. A gate stack 314 is formed on the substrate 302 over the channel region 312. The gate stack includes an oxide layer 316, polysilicon layer 318, silicide layer 320, oxide layer 322, and nitride passivation layer 324 formed as shown. The layers 316-324 in the gate stack 314 result in the stack having a height H, and the contacts 304, 306 are formed having at least the height H to enable reliable connection to the contacts via subsequently formed layers. An insulating spacer layer 326, such as a silicon nitride or silicon oxide layer, is disposed on both sides of the gate stack 314 between the gate stack and the contacts 304, 306 to isolate the conductive layers in the stack from the contacts. In operation, a gate voltage is applied to the polysilicon layer 318 to induce a channel in the channel region 312, causing current to flow through the contact 306, through the drain region 310 and through the channel region to the source region 308, and through the source region to the contact 304, as will be appreciated by those skilled in the art. --

In the Claims:

Please cancel claims 1-29, amend claims 31, 33 and 35, and add new claims 37-51 as follows:

31. (Amended) The integrated circuit of claim 30 wherein the integrated circuit comprises a dynamic access random memory.

33. (Amended) The integrated circuit of claim 32 wherein the control stack of each MOS transistor comprises a gate stack including an oxide layer, polysilicon layer, silicide layer, another oxide layer, and a nitride layer.

35. (Amended) The integrated circuit of claim 34 wherein the electromagnetic radiation comprises collimated light.

-- 37. (New) The integrated circuit of claim 30 wherein an insulating spacer layer is disposed between the control stack and the contacts.

38. (New) An in-process substrate structure including a plurality of contact regions and a plurality of non-contact regions adjacent the contact regions on an upper surface of the substrate, the in-process substrate structure comprising:

a contact formed on each contact region, each contact having a top surface and two sidewall surfaces disposed between the top surface and the upper surface of the substrate, the top surface being heated to increase a vertical growth rate of the contact relative to a horizontal growth rate of the contact so that each sidewall remains substantially vertical and overlap of the contact into adjacent non contact regions due to lateral growth is limited.

39. (New) The substrate of claim 38 wherein the top surface is substantially parallel to the upper surface of the substrate.

40. (New) The substrate of claim 38 wherein the top surface is substantially horizontal.

41. (New) The substrate of claim 38 wherein the contact is heated by illuminating an upper surface of the contact with electromagnetic radiation.

42. (New) The substrate of claim 41 wherein the electromagnetic radiation comprises collimated light.

43. (New) The substrate of claim 42 wherein the collimated light comprises a scanning laser beam.

44. (New) The substrate of claim 42 wherein the collimated light is propagated substantially perpendicular to the top surface of the contact.

45. (New) The substrate of claim 38 wherein the non-contact regions adjacent to the contact region comprise isolation oxide regions.

46. (New) The substrate of claim 38 wherein the substrate comprises silicon.

47. (New) The substrate of claim 38 wherein the substrate comprises gallium arsenide.

48. (New) The substrate of claim 38 wherein the substrate comprises silicon germanium.

49. (New) The substrate of claim 38 wherein the contact comprises silicon.

50. (New) The substrate of claim 38 wherein the contact comprises gallium arsenide.

51. (New) The substrate of claim 38 wherein the contact comprises silicon germanium. --

REMARKS

The Examiner is requested to enter the above amendments before commencing examination of the present patent application.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made"**.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at line 13 of page 2 has been amended as follows:

The lateral growth 118 may result in adjacent contacts undesirably touching each other, as indicated by the dotted lines 122 between the contacts 100 and 102. When the contacts 100 and 102 touch, an unwanted short circuit occurs and the devices being fabricated may not operate properly. As the size of devices being formed in integrated circuits continues to decrease, the distance between adjacent contacts 100, 102 and 102, 104 also decreases, making lateral growth 118 a concern since less lateral growth is required before adjacent contacts short circuit. While the amount of lateral growth of the contacts 100-104 can be reduced by forming the contacts for a shorter period of time, this is not a viable in most applications because the contacts must be formed to a desired height H, as indicated for the contact 100. As will be appreciated by those skilled in the art, the contacts 100-104 must reach the desired height H, for example, in order to ensure subsequent layers (not shown) can reliably connect to the contacts to provide electrical connection to the underlying devices. For example, in a MOS transistor [contacts] it is desirable that contacts being formed to source and drain regions of the transistor are at least as high as a gate stack formed over a channel region of the transistor to ensure subsequent layers form proper connection to the contacts.

Paragraph beginning at line 5 of page 5 has been amended as follows:

During the selective formation of the contacts 200-204, the collimated electromagnetic radiation 208 is applied to the contacts to heat the horizontal upper surfaces of the contacts, as will be now described in more detail with reference to the contact 202. The contact 202 includes an upper surface 220 that is substantially horizontal or parallel to the upper surface on the silicon substrate 206, and further includes two sidewall surfaces 222 and 224 that are substantially vertical or perpendicular to the upper surface of the silicon substrate. The collimated electromagnetic radiation 208 has a direction of propagation, as indicated by the

arrows, which is substantially perpendicular to the surface of the semiconductor substrate 206 and the upper surface 220. A scanning laser or other suitable source [maybe]may be utilized to generate the collimated electromagnetic radiation 208, and although the radiation is described as being electromagnetic radiation, any directional radiation source that can heat the upper surface 220 by a relatively large amount compared to the sidewall surfaces 222, 224 can be utilized, as will be discussed in more detail below.

Paragraph beginning at line 20 of page 5 has been amended as follows:

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Paragraph beginning at line 17 of page 7 has been amended as follows:

Figure 3 is a diagram illustrating a MOS transistor 300 formed in a semiconductor substrate 302, the MOS transistor including contacts 304, 306 formed according to the method of Figure 2. In the example of Figure 3, the MOS transistor is an NMOS device including an N+ source region 308 and N+ drain region 310, with a P-type channel 312 being defined between the source and drain regions. A gate stack 314 is formed on the substrate 302 over the channel region 312. The gate stack includes an oxide layer 316, polysilicon layer 318, silicide layer 320, oxide layer 322, and nitride passivation layer 324 formed as shown. The layers 316-324 in the gate stack 314 result in the stack having a height H, and the contacts 304, 306 are formed having at least the height H to enable reliable connection to the contacts via subsequently formed layers. An insulating spacer layer 326, such as a silicon nitride or [silicone]silicon oxide layer, is disposed on both sides of the gate stack 314 between the gate stack and the contacts 304, 306 to isolate the conductive layers in the stack from the contacts. In operation, a gate voltage is applied to the polysilicon layer 318 to induce a channel in the channel region 312, causing current to flow through the contact 306, through the drain region 310 and through the channel region to the source region 308, and through the source region to the contact 304, as will be appreciated by those skilled in the art.

In the Claims:

Claims 1-29 have been cancelled.

Claims 31, 33 and 35 have been amended as follows:

31. (Amended) The integrated circuit of claim 30 wherein the integrated circuit comprises a[n] dynamic access random memory.

33. (Amended) The integrated circuit of claim 32 wherein the control stack of each MOS transistor comprises a gate stack including an oxide layer, polysilicon layer, silicide layer, another oxide layer, and a nitride layer.

35. (Amended) The integrated circuit of claim 34 wherein the electromagnetic radiation comprises collimated light.

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